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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/939,253	08/24/2001	James M. Derderian	4830US (01-0106)	2189

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EXAMINER	
WILLIAMS, ALEXANDER O	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 05/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/939,253	DERDERIAN, JAMES M.	
	Examiner	Art Unit	
	Alexander O Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Peri d for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-67* is/are pending in the application.

4a) Of the above claim(s) *14 to 16, 27 to 30, 34 to 36, 41 and 48 to 67* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 to 13, 17-26, 31 to 33, 37 to 40 and 42 to 44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 09/939253 Attorney's Docket #: 4830US(01-0106)
Filing Date: 8/24/01;

Applicant: Derderian

Examiner: Alexander Williams

Applicant's Amendment filed 2/24/04 have been acknowledged. The claims being examined are claims 1 to 13, 17-26, 31 to 33, 37 to 40 and 42 to 44.

This application contains claims 14 to 16, 27 to 30, 34 to 36, 41 and 48 to 67 drawn to an invention non-elected without traverse in Paper No. 11.

Claims 68 to 102 have been canceled.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 to 10, 17, 19 to 26, 33, 40 and 42 to 44 are rejected under 35 U.S.C. § 102(e) as being anticipated by Foster (U.S. Patent # 6,552,416 B1).

For example, in claim 1, Foster (figures 1 to 10c) specifically figure 8 show a semiconductor device for use in a stacked multi-chip assembly, comprising: a semiconductor die **31**; and a dielectric spacer layer **32** formed on and secured to (by 20 and lower 33) at least a portion of a surface of said semiconductor die (by 20 and lower 33) and protruding from the surface substantially a predetermined distance that said semiconductor die and an adjacent semiconductor die **30** of said stacked multi-chip assembly are to be spaced apart from one another, said spacer layer including voids **(in figure 8, middle portion between the two stacks of 33 and 20s)** communicating with a lateral periphery thereof.

For example, in claim 19, Foster (figures 1 to 10c) specifically figure 8 show a semiconductor device assembly, comprising: a first semiconductor device **31**; a nonconfluent spacer layer **32** comprising dielectric material secured to a surface of said first semiconductor device, a second semiconductor device **30** positioned over said first semiconductor device, a surface of said second semiconductor device being secured to said nonconfluent spacer layer.

Claims 1 to 10, 13, 17, 19 to 26, 32, 33, 37 to 40 and 42 to 44 are rejected under 35 U.S.C. § 102(e) as being anticipated by Shim et al. (U.S. Patent # 6,531,784 B1).

For example, in claim 1, Shim et al. (figures 1 to 11) specifically figure 8 show a semiconductor device for use in a stacked multi-chip assembly, comprising: a semiconductor die **14**; and a dielectric spacer layer **50A,50C** formed and secured to on at least a portion of a surface of said semiconductor die and protruding from the surface substantially a predetermined distance that said semiconductor die and an adjacent semiconductor die **16** of said stacked multi-chip assembly are to be spaced apart from one another, said spacer layer including voids **(in figure 8, middle portion between the two 50A,50Cs)** communicating with a lateral periphery thereof.

For example, in claim 19, Shim et al. (figures 1 to 11) specifically figure 8 show a semiconductor device assembly, comprising: a first semiconductor device **14**; a nonconfluent spacer layer **50A,50C** comprising dielectric material secured to on a surface of said first semiconductor device, a second semiconductor device **16** positioned over said first semiconductor device, a surface of said second semiconductor device being secured to said nonconfluent spacer layer.

In claim 37, Shim et al. (figures 1 to 11) specifically figure 8 show a substrate **12** upon which one of said first semiconductor device **14** and said second semiconductor device **16** is positioned.

In claim 38, Shim et al. (figures 1 to 11) specifically figure 8 show at least one bond pad **(inherit in figure 8, shown as 58 in figure 9)** of at least one of said first semiconductor device and said second semiconductor device **31** is in communication **(through 28B)** with a corresponding contact area **22** of said substrate **12.**

In claim 39, Shim et al. (figures 1 to 11) specifically figure 8 show the substrate comprising at least one of a circuit board **12**, an interposer, another semiconductor device, and leads.

Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shim et al. (U.S. Patent # 6,531,784 B1) in view of Smith, Jr. et al. (U.S. Patent # 6,049,370).

Shimi et al. show the features of the claimed invention as detailed above, but fail to explicitly show a spacer layer comprising polymer, where as the polymer comprises a photoimageable polymer. Shimi does discloses that the jumper strips 50A, 50B, and 50C can be made of a variety of insulative materials and by a variety of techniques. For example, they can be fabricated from a resin tape or a sheet of fiberglass impregnated with an epoxy resin using conventional circuit tape or PCB fabrication techniques. Photoimageable polymer is defined to be a photoresist polymer.

Smith,Jr. et al. is cited for showing liquid crystal light valvue using internal, fixed spacers. Specifically, Smith, Jr. et al. (figures 2 to 5) specifically figure 3 discloses a ariety of materials may be used to form the spacer pads 40, including an oxide, such as silica or indium tin oxide, a metal, such as chromium, aluminum, or gold, and polymers, such as polyimides or photoresist materials for the purpose of giving spacing between electrical connecting materials.

Therefore, it would have been obvious to one of ordinary skill in the art to use Smith, Jr. et al.'s photoresist polymer spacer to modify Shim et al.'s spacers for the purpose of giving spacing between electrical connecting materials.

Claims 18 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shim et al. (U.S. Patent # 6,531,784 B1) in view of Blanton (U.S. Patent # 5,220,200).

Initially, it is noted that the 35 U.S.C. § 103 rejection based on a dielectric spacer layer and a plurality of at least partially superimposed, contiguous, adhered sublayers deals with an issue (i.e., the integration of multiple pieces into one piece or conversely, using multiple pieces in replacing a single piece) that has been previously decided by the courts.

In Howard v. Detroit Stove Works 150 U.S. 164 (1893), the Court held, "it involves no invention to cast in one piece an article which has formerly been cast in two pieces and put together...."

In In re Larson 144 USPQ 347 (CCPA 1965), the term "integral" did not define over a multi-piece structure secured as a single unit. More importantly, the court went further and stated, "we are inclined to agree with the solicitor that the use of a one-piece construction instead of the [multi-piece] structure disclosed in Tuttle et al. would be merely a matter of obvious engineering choice" (bracketed material added). The court cited In re Fridolph for support.

In re Fridolph 135 USPQ 319 (CCPA 1962) deals with submitted affidavits relating to this issue. The underlying issue in In re Fridolph was related to the end result of making a

multi-piece structure into a one-piece structure. Generally, favorable patentable weight was accorded if the one-piece structure yielded results not expected from the modification of the two-piece structure into a single piece structure. Shim et al. dielectric layer can be a plurality of at least partially superimposed, contiguous, adhered sublayers.

Blanton is cited for showing provision of substrate pillars to maintain chip standoff. Specifically, Blanton (figures 1 to 3) specifically figure 3 discloses dielectric layer can be a plurality of at least partially superimposed, contiguous, adhered sublayers for the purpose of providing standoff means to space an integrated circuit.

Therefore, it would have been obvious to one of ordinary skill in the art to use the dielectric spacer layer and a plurality of at least partially superimposed, contiguous, adhered sublayers as "merely a matter of obvious engineering choice" as set forth in the above case law. However, it would have been obvious to one of ordinary skill in the art to use Blanton's series of layer to make a spacer to modify Shim et al.'s spacers for the purpose of providing standoff means to space an integrated circuit.

Claims 11, 13 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Foster (U.S. Patent # 6,552,416 B1) in view of Mueller et al. (U.S. Patent # 6,316,786 B1).

Foster show the features of the claimed invention as detailed above, but fail to explicitly show a spacer layer comprising (all types) at least one of a glass, a silicon oxide, a silicon nitride, and a silicon oxynitride.

Mueller et al. is cited for showing an organic opto-electronic devices. Specifically, Mueller et al. (figures 1A to 3c) specifically figure 1B discloses spacers 13 and 15 comprising silicon nitride, SiN.sub.x, SiO.sub.x, SiO.sub.2, Siliconoxynitride (SiON), organic compounds such as polyimides, aluminiumoxide, aluminiumnitride, or titaniumoxide, for example for the purpose of providing sufficient contact between the layers and damage between the layers are avoided.

Therefore, it would have been obvious to one of ordinary skill in the art to use Mueller et al.'s spacer to modify Foster's spacers for the purpose of providing sufficient contact between the layers and damage between the layers are avoided.

Response

Applicant's arguments filed 2/24/04 have been fully considered, but are moot in view of the new grounds of rejections detailed above.

The insertion of Applicant's additional claimed language, for example, "in claims 1 and 19, " cause for further search and consideration to make this action final.

Applicant's amendment necessitated the new grounds of rejection. Accordingly, **THIS ACTION IS MADE FINAL**. See M.P.E.P. § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. § 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION A0ND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. § 1.136(a) WILL BE CALCULATED FROM THE

MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

Field of Search	Date
U.S. Class and subclass: 257/686,685,777,778,784-787,734,737,738,723,730,773	9/9/02 2/22/03 5/8/03 8/18/03 11/17/03 5/4/04
Other Documentation: foreign patents and literature in 257//686,685,777,778,784-787,734,737,738,723,730,773	9/9/02 2/22/03 5/8/03 8/18/03 11/17/03 5/4/04
Electronic data base(s): U.S. Patents EAST	9/9/02 2/22/03 5/8/03 8/18/03 11/17/03 5/4/04

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AOW
5/4/04

Alexander Williams
Primary Examiner